WHAT IS CLAIMED IS:

1. A method of fabricating a semiconductor integrated circuit device, comprising the steps of:

(a) performing a wafer process to a plurality of wafers, thereby forming a plurality of semiconductor integrated circuit devices over each of the wafers;

(b) after step (a), performing a first electrical test to a first set of wafers selected from the plurality of wafers accommodated in a first wafer cassette placed in a wafer prober; and

(c) after step (a), performing a second electrical test to a second set of wafers selected from the plurality of wafers accommodated in a second wafer cassette placed in the wafer prober by automatically changing a test object to the second set of wafers.

2. The method according to claim 1, wherein the first electrical test and the second electrical test are substantially the same test.

3. The method according to claim 2, wherein the first wafer set and the second wafer set are substantially the same product typed wafers.

4. A method of fabricating a semiconductor integrated circuit device, comprising the steps of:

(a) performing a wafer process to a plurality of wafers, thereby forming a plurality of semiconductor integrated circuit devices over each of the wafers;

(b) after step (a), performing a first electrical test to a first set of wafers selected from the plurality of wafers accommodated in a first wafer cassette placed in a wafer prober; and

(c) in step (b), performing checking of image data of probing needle traces of the wafer prober.

5. The method according to claim 4, wherein in the step (b), a probing position of the wafer prober is corrected on the basis of the result of having checked the probe trace image data.

6. The method according to claim 5, wherein the electrical test is a probe check.

7. A method of fabricating a semiconductor integrated circuit device, comprising the steps of:

(a) performing a wafer process to a plurality of wafers, thereby forming a plurality of semiconductor integrated circuit devices over each of the wafers;

(b) after step (a), performing a first electrical test with a first test program to a first set of wafers selected from the plurality of wafers accommodated in a first wafer cassette placed in a wafer prober; and

(c) after step (a), performing a second electrical test with a second test program to a second set of wafers selected from the plurality of wafers accommodated in a second wafer cassette placed in the wafer prober by automatically changing a test program from the first test program to the second test program.

8. The method according to claim 7, wherein the second electrical test is performed by automatically changing a test object to the second set of wafers.

9. The method according to claim 8, wherein the electrical test is a probe